

PCB Hints and Tips

Many designers are unaware of the basic process involved in PCB manufacture which can lead to misconceptions as to what can be done and what can't, what's expensive and what's not.

Process flow for double sided plated boards

Material selection: Typically, this is FR4 (Flame Retardant Epoxy Woven Glass) with 0.5oz (17uM) copper cladding glued to both sides although there are many other options available with different substrates and different copper thicknesses.

Drilling: For plated holes we apply "drill compensation" which means that holes are drilled oversize but when plated (at a later stage) the finished hole size matches the customer's specification. For this reason, your instructions should specify finished holes size rather than drill size.

Phototool preparation: The phototools for tracking have to be manipulated to achieve the desired result (known as "etch compensation"). For example, if the desired track width is 10thou and assuming base copper of 1oz then the phototool track width would be 10.5thou. Because of undercutting during the subsequent etch process the result would be approximately 10thou. If the copper weight is heavier than 35uM then more compensation would be necessary and vice versa.

Plating: Various methods are possible but the end results are the same i.e. we have plating on the track pattern and inside the drilled holes but not on the areas between tracks. The thickness of the plating is controllable but is normally usually specified as 20uM minimum.

Etching: Again, various methods are possible but the result is that the track pattern is preserved and unwanted copper removed.

Solder mask are applied at this stage, normally green

Finishing: Exposed tracks and pads are finished in a variety of methods, the most common being LFHASL (Lead-Free Hot Air Solder Levelled) or ENIG (Electro Nickel Gold). Circuit areas covered by solder mask are unaffected.

Legend are applied at this stage, normally white or yellow

Profiling: Circuits are normally panelised for production. The main methods to support subsequent separation into singles are routing, scoring or a combination of the two.

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How to reduce costs:

- Use standard materials eg FR4 in 1.6mm, 1.2mm, 1.0mm, 0.8mm where possible
- Avoid fine routing ie tool size < 1.6mm
- Avoid fine holes ie <0.3mm
- Follow these basic specifications for OUTER or INNER layers:
 - For 17uM (1oz) base copper design to minimum track/space of 4/4thou
 - For 35uM (1oz) base copper design to minimum track/space of 6/6thou
 - For 70uM (2oz) base copper design to minimum track/space of 10/10thou
- LFHASL is cheaper than ENIG but is considered inadequate for fine pitch devices
- Accept panels with faulty circuits (AKA X-outs) where possible
- Don't let your assembler insist on large panel borders for their convenience. Border areas (scrap) are charged at the same rate as circuit area. Example: circuit area 100 x 100mm, 4 up on panel with no spaces between and no borders. Circuit cost would be based on 100mm². Adding 4 borders at 10mm increases the panel area by 21% and hence the circuit cost by 21%. Adding 4 borders at 20mm increases the panel area by 44% and hence the circuit cost by 44%.
- Avoid chamfered and rebated holes.
- Optimise circuit profile to allow scoring. Scoring is cheap, produces stronger panels during assembly but is less accurate than routing. At least 20thou of space must be kept clear of copper and components along any scored edge.
- Optimise circuit profile so circuits can be butted together without space between. Space between circuits is charged at the same rate as the circuit.
- Making profiles symmetrical can frequently save panelisation wastage.
- Avoid profiles needing support by chain-drilled slots. They can look untidy, take time to separate and make a lot of dust if finishing is required.
- See separate section herein concerning profile optimisation.

What can't be done:

- Copper weights must be the same on top and bottom layers.
- Etching becomes more difficult as copper weight increases (see above about etch compensation). Essentially, fine track/space and thick copper are mutually exclusive because of process constraints.
- Solder mask slivers (the mask remaining between pads) must be minimum 4thou. A minimum of 2 thou annulus around the copper pad is required to avoid leaching onto the copper ie a copper pad at 20thou needs a solder mask pad of 24 thou minimum. It follows that the minimum pad to pad space must be 8thou. Some CAD footprints leave less than 8thou which can result in the factory removing the sliver altogether resulting in no mask between the pads at all. Under such circumstances you might consider changing a 12thou pad to – say – 11 thou.
- Overplating (ie more than 20uM) is not a good idea for SMD boards because it leads to rounding of the pad section which in turn leads to assembly problems because of reduced solder volume.

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Good practice:

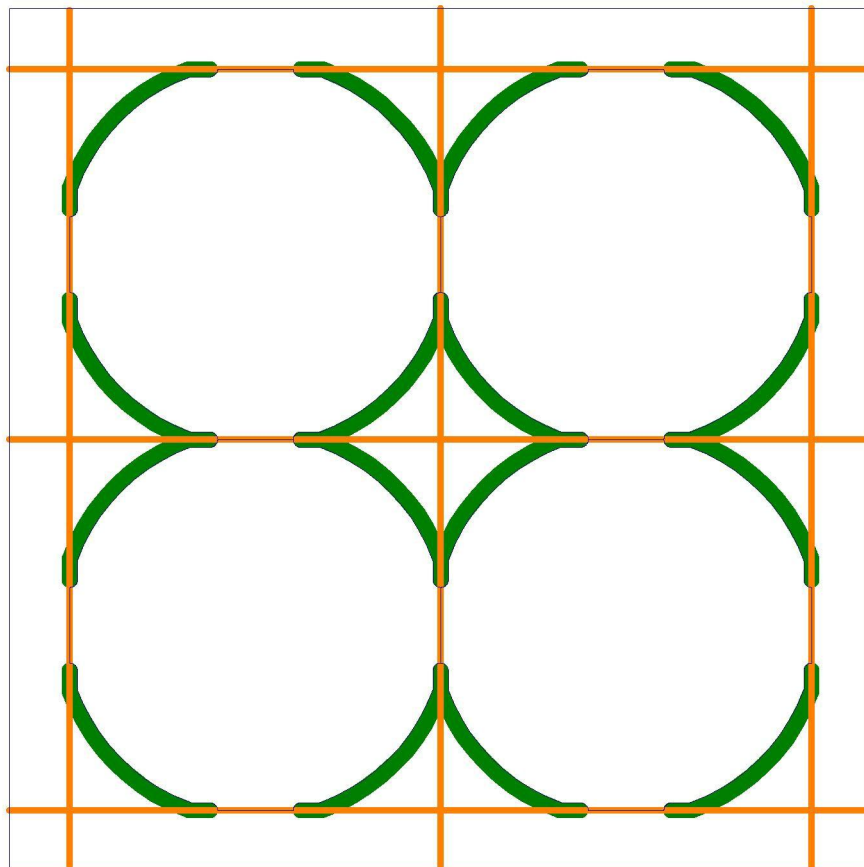
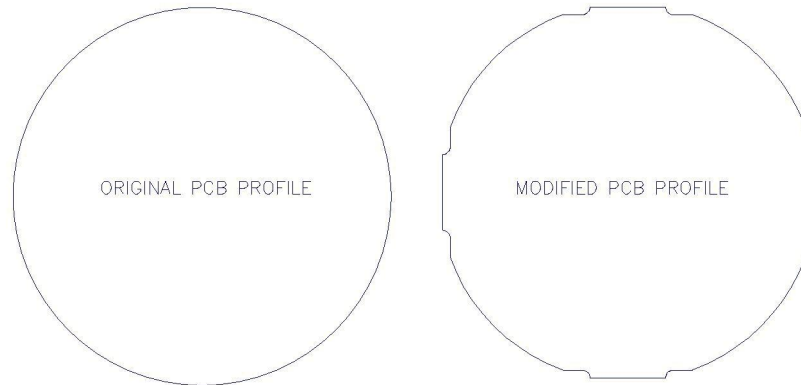
- Let your factory have as much supporting info as possible but do not duplicate. Multiple sources of information can be as much of a problem as missing information. At least, send a README covering the basic requirements such as material, copper weight (specify base (preferred) or finished but not both), mask and legend colours, finish, non plated holes, critical radii, critical tolerances but also document anything unusual or things that may not be obvious from the data itself.
- Produce gerbers and drill files with the same degree of accuracy and in same units. Imperial or metric is fine but a mixture is not. Many CAD systems default to producing manufacturing files in 2.3 English (Imperial) format which means two digits before the decimal place and three after. This is inadequate for fine pitch devices and the subsequent rounding will produce uneven spaces between pads. Solder mask may be affected (see above). In-house, we specify everything in 2.5 English, both gerber and drill.
- Consider using ODB++ files if possible. These contain much more information than gerber and drill files.
- If using CAD auto routing, don't let the system track everything to the minimum clearances. Manually track if necessary.
- Ensure the circuit profile is shown as a complete line and in nominal width. Industry protocol is to regard the centre of the line as the actual profile.
- Add text either inside or outside the circuit profile to indicate the layer number. This is especially important on double sided non-SMD boards and multi-layers.
- Send solder mask data at copper pad plus zero annulus ie copper pad and mask pad are the same size. Leave it to us to adapt the mask as appropriate.

Profile optimisation for economy:

The following pages shows some examples of how profiles can be modified to promote:

- Material yield (to reduce cost)
- Panel structural strength (to ensure we can handle the panels safely)
- Ease of circuit separation (to reduce cost and minimise clean-up). A mix of scoring and routing is normal.

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EXAMPLE SHOWING CIRCULAR PCB WITH ADDED FLATS TO AID MANUFACTURING

BLUE = CIRCUIT PROFILE
ORANGE = SCORE LINES
GREEN = ROUTE LINES (2MM TOOL)

BENEFITS:

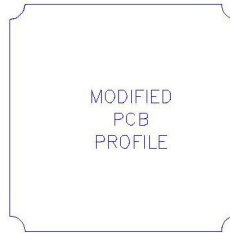
- 1) MUCH IMPROVED MATERIAL YIELD
- 2) MUCH MORE RIGID DURING ASSEMBLY
- 3) LEAVES NO CHAIN DRILLED NUBS TO BE SANDED



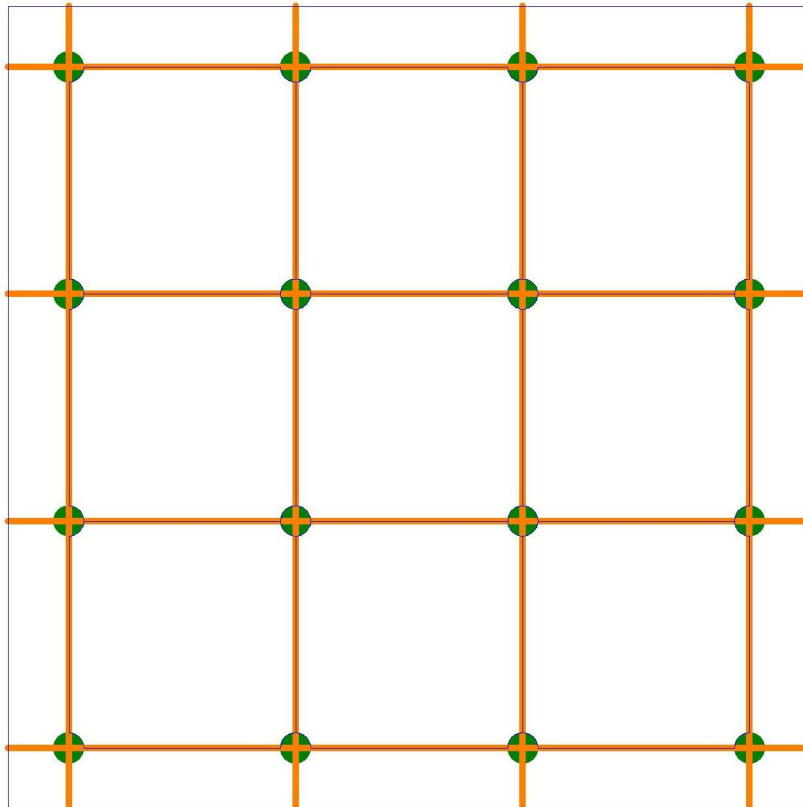
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ORIGINAL
PCB
PROFILE



MODIFIED
PCB
PROFILE



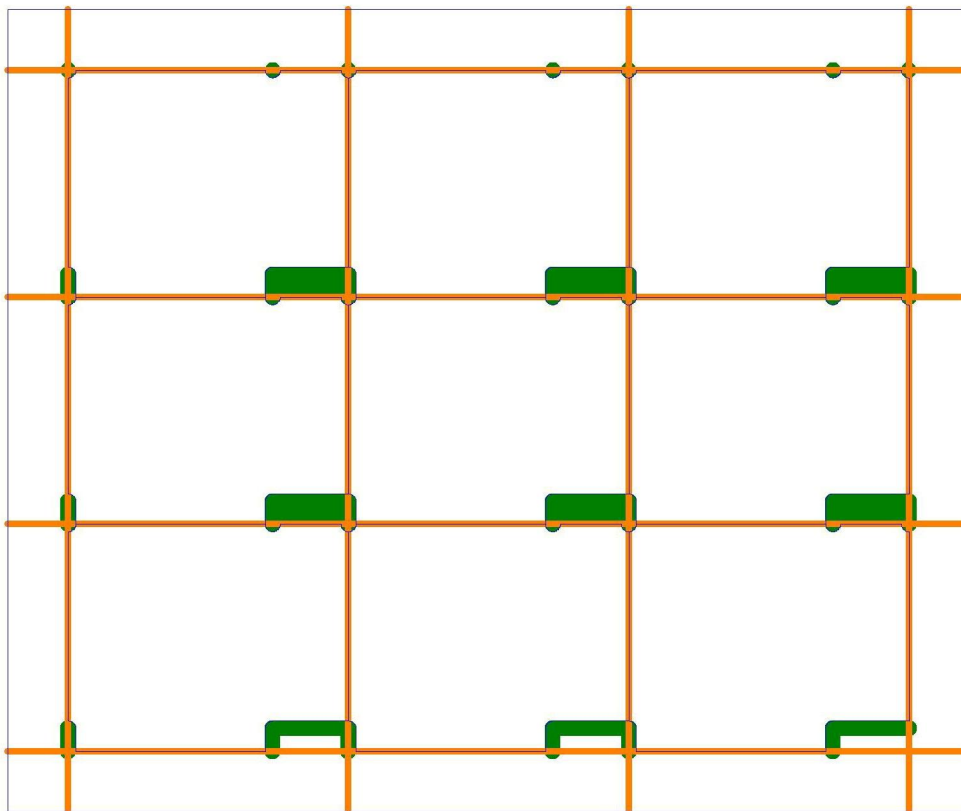
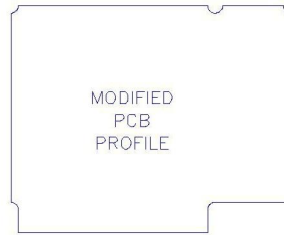
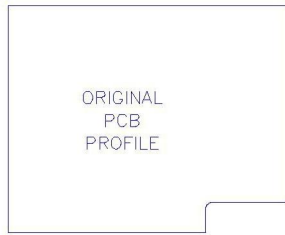
CHAMFERED CORNERS FORCE SPACE TO BE LEFT BETWEEN CIRCUITS

INDENTED ROUNDS ALLOW CIRCUITS TO ABUTTED AND SCORED

BLUE = CIRCUIT PROFILE
ORANGE = SCORE LINES
GREEN = ROUTE LINES (2MM TOOL)



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ASYMMETRICAL SHAPES FORCE SPACE TO BE LEFT BETWEEN CIRCUITS

INDENTED ROUNDS ALLOW CIRCUITS TO ABUTTED AND SCORED

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 GREEN = ROUTE LINES (2MM TOOL)